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Performance comparison between CNFET & Conventional CMOS based Arithmetic Logic Unit

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Abstract

This paper presents the implementation and analysis of Carbon Nano tube Field Effect transistor (CNFET) and CMOS based one bit ALU .It is well known that the ALU is the key component of any processor. The functioning of the processor depends partially or as a whole on its ALU. Therefore there is a need to design ALUs with high efficiency and reliability. CNFET is used for high performance, high stability and low-power circuit designs as an alternative material to silicon in recent years. Hspice based results demonstrate that the CNFET based ALU circuits achieve great improvement in terms of power dissipation with respect to their CMOS counterpart at 10 nm Technology.

Keywords: CNFET, ALU, 10 nm technology, Hspice, low power.

Introduction

CNFETs are similar to MOSFETs except that their conducting channel is made of CNT instead of bulk silicon.

Carbon nanotubes (CNTs) are allotropes of carbon with a cylindrical Nano structure. These are quasi-one-dimensional molecular structures and can be considered as a result of folding graphite (a hexagonal lattice of carbon) layers into cylinders [1] [2]

They exhibit extraordinary strength and unique electrical properties, and are efficient conductors of heat [1].

With technological advances, there is a need to pack an increasing number of transistors in an IC of given area so as to obtain high efficiency with respect to speed, power consumption, delay etc. This can be done by the scaling down of transistors. But off late, scaling down of CMOS devices is bound to arrive at its end [3] [4] due to disadvantages such as short channel effects, drain induced barrier lowering (DIBL), hot electrons etc. [3] As the CMOS devices approach fundamental limits on size, CNFET proves to be a promising alternative for low power and high performance devices, owing to low off-current and ballistic transport [4].

ALU is the heart of any processor and is a part that is designed first. It performs basic arithmetic and logical operations. The efficiency of a processor greatly depends on the ALU [5]. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications [5]. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing application [5].

The ALU which we have implemented performs arithmetic operations such as addition & subtraction and logical operations such as AND & OR.

CNFET based Logic Circuits

The first logic circuits with field-effect transistors based on single carbon nanotubes were built as resistive load circuits [6].One, two, and three-transistor circuits were demonstrated experimentally to exhibit a range of digital logic operations such as NAND gate, NOR gate, inverter etc. [6] CNFET based devices offer high mobility, ballistic transport, high carrier velocity for fast switching, due to the quasi-one-dimensional structure of CNTs [7].

These advantages of CNFET have been exploited to design logic circuits in order to satisfy the need for high speed processing.

ALU Design

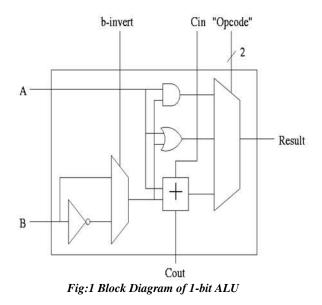
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The ALU which we have implemented performs arithmetic operations such as addition & subtraction and logical operations such as AND & OR.

In the 1-bit ALU shown in fig:1, the logical operations are performed by the 2 input AND & OR gate while the arithmetic operations are performed by the full adder. The full adder performs addition or subtraction depending upon the select line b-invert of the 2:1 multiplexer. To implement addition, we disable b-invert whereas to perform subtraction b-invert is enabled.



In order to perform subtraction using an adder; one of the inputs has to be in 2's complement form. i.e. The input has to be in $A + (\sim B + 1)$ form. The +1 is obtained from Cin. The output Cout of the full adder indicates the carryout in case of addition. The 2-bit opcode selects the result of either logical or arithmetic block which will be the output of the ALU. The following table2, summarizes the select lines and operations performed by the ALU.

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Table 2: Alu Operation

b-invert	opcode	operation
0	00	AND
0	01	OR
0	10	ADD
1	10	SUB

Results and Discussions

The one- bit ALU based on CNTFET is implemented and analyzed at 10nm technology. Another one-bit ALU based on MOSFET at 10nm technology is also implemented and analyzed for comparison, both sharing the same design. This circuit is simulated in HSPICE using Stanford CNTFET model at 10nm feature size with supply voltage VDD of 0.9V.

The following technology parameters are used for simulation using CNTFET Technology : Physical channel length (L channel) = 32.0nm

The length of doped CNT source/drain extension region $(L_sd) = 32.0$ nm

Fermi level of the doped S/D tube (Efo) = 0.6 eV

The thickness of high-k top gate dielectric material (Tox) = 4.0nm

Chirality of tube (m, n) = (19, 0)

CNT Pitch = 10nm

Flatband voltage for n-CNTFET and p-CNTFET (Vfbn and Vfbp) = 0.0eV and 0.0eV

The mean free path in intrinsic CNT (Lceff) = 200.0nm

The mean free path in p+/n+ doped CNT = 15.0nm

The work function of Source/Drain metal contact = 4.6eV

CNT work function = 4.5 eV

|--|

Technology	MOSFET(10n)	CNFET(10n)
Total voltage	1.204e-05	1.001e-06
source power	watts	watts
dissipation		

The one dimensional nature of CNTs reduces the phase space for scattering allowing CNTs to realize maximum possible bulk mobility of this material[13]. low scattering together with the strong chemical bonding and high thermal conductivity allows CNTs to withstand extremely high current densities, thus CNFET has low power dissipation than the MOSFET's.

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Conclusion

From an economic point of view, conventional devices and materials will continue to be employed until they become impractical. Carbonbased devices show promising features, so that they are considered as potential candidates to replace silicon based MOSFETs in the future. In this paper a one-bit ALU is implemented using CNTFETs at 10nm Technology to reduce power dissipation. This CNTFET based one-bit ALU circuit is compared to conventional MOSFET based one-bit ALU for performance comparison analysis. These circuits are simulated using HSPICE and the results are tabulated in table 1. The results shows that the Power Dissipation of CNFET based ALU is reduced by approximately 92% compared to MOSFET based ALU.

References

- [1] Design & Simulation of carbon nanotube based logic circuit (inverter) for advance applications published International Journal of Electrical, Electronics & Communication Engineering, Vol. 2No. 10thOctober 2012
- [2] Cho, Geunho, Yong-Bin Kim, and Fabrizio Lombardi. "Assessment of CNTFET based circuit performance and robustness to PVT variations." Circuits and Systems, 2009. MWSCAS'09. 52nd IEEE International Midwest Symposium on. IEEE, 2009.
- [3] Haselman, Michael, and Scott Hauck. "The future of integrated circuits: A survey of nanoelectronics." Proceedings of the IEEE 98.1 (2010): 11-38.
- [4] Das, Subhajit, Sandip Bhattacharya, and Debaprasad Das. "Design of Digital Logic Circuits using Carbon Nanotube Field Effect Transistors." International Journal of Soft Computing and Engineering 1.6 (2011): 173-178.\
- [5] Krishna, V. Vamshi, and S. Naveen Kumar. "High Speed, Power and Area efficient Algorithms for ALU using Vedic Mathematics." International Journal of Scientific and Research Publications 2.7 (2012).
- [6] CNTFET based Logic Circuits: A Brief Review Sinha, Sanjeet Kumar, and Saurabh Choudhury. "CNTFET based Logic Circuits: A Brief Review." Int. J. Emerging Technol. Adv. Eng 2.4 (2012): 500-504.
- [7] J. Deng et al., "Carbon nanotube transistor circuits: Circuit-level performance benchmarking and design options for living

Scientific Journal Impact Factor: 3.449 (ISRA), Impact Factor: 1.852

with imperfections," in Proc. Intl. Solid-State Circuits Conference, pp. 70–588, 2007.

- [8] Huddar, Sushma R., et al. "Area and Speed Efficient Arithmetic
- [9] Logic Unit Design Using Ancient Vedic Mathematics on FPGA." Advances in Computing, Communication, and Control. Springer Berlin Heidelberg, 2013. 475-483.
- [10]Anand, Aparna, and S. R. P. Sinha. "Performance Evaluation of Logic Gates Based On Carbon Nanotube Field Effect Transistor." International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-2, Issue-5, November 2013
- [11]International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.4, December 2011 DOI : 10.5121/vlsic.2011.2414 167 Design of low write-power consumption sram cell based on cnfet at 32nm technology Rajendra Prasad S1, Prof. B K Madhavi2 and Prof. K Lal Kishore3 1Department of ECE, ACE Engineering College, Hyderabad, AP, India.
- [12]A. Bachtold, P. Hadley, T. Nakanishi, C. Dekker 2001, Logic Circuits with Carbon Nanotube Transistors, Science, vol. 294, no. 9 pp. 1317-1320, November 2001.

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